THE INVENTION CLAIMED IS:

1. A process for sputter depositing a barrier layer on a bottom and sidewalls of a via defined in a dielectric layer over a copper feature of a semiconductor substrate disposed on a support pedestal in a sputter deposition chamber having a sputtering target and an RF coil for coupling RF energy to a plasma maintained between the sputtering target and the support pedestal, the process comprising the steps of:

(a) sputter depositing a barrier layer onto the sidewalls and bottom of the via by applying power to at least the sputtering target and the support pedestal; and

(b) reducing a thickness of the barrier layer on the bottom of the via by applying power to at least the RF coil and the support pedestal.

2. The process of claim 1 wherein steps (a) and (b) are performed simultaneously.

3. The process of claim 1 wherein step (b) includes applying power to the target.

4. The process of claim 3 wherein steps (a) and (b) comprise adjusting a level of power applied to the target, a voltage level and duty cycle applied to the support pedestal and an RF power applied to the RF coil so as to sputter deposit the barrier layer onto the sidewalls and bottom of the via and sputter etch the barrier layer from the bottom of the via.

5. The process of claim 1 wherein step (a) includes applying power to the RF coil.

6. The process of claim 1 wherein steps (a) and (b) are performed sequentially.

7. The process of claim 1 wherein depositing a barrier layer comprises depositing at least one of tantalum and tantalum nitride.

8. A process for sputter depositing a barrier layer on a bottom and sidewalls of a via defined in a dielectric layer over a copper feature of a semiconductor substrate disposed on a support pedestal in a sputter deposition chamber having a sputtering target and an RF coil for coupling RF energy to a plasma maintained between the sputtering target and the support pedestal, the process comprising the steps of:

(a) sputter depositing a barrier layer onto the sidewalls and bottom of the via by applying power to at least the sputtering target and the support pedestal; and

(b) exposing at least a portion of the copper feature by sputtering both the barrier layer on the bottom of the via and any copper oxide layer on at least a portion of the copper feature by applying power to at least the RF coil and the support pedestal.

9. The process of claim 8 wherein depositing a barrier layer comprises depositing at least one of tantalum and tantalum nitride.

10. A process for deposition of copper within a via having sidewalls and a bottom defined in a dielectric layer over a copper feature, comprising:

in a high density plasma deposition chamber coupled to a transfer chamber, performing the steps of:

depositing a barrier layer on the sidewalls and bottom of the via; and

reducing a thickness of the barrier layer on the bottom of the via by sputtering the barrier

layer on the bottom of the via;

transferring the substrate from the high density plasma deposition chamber to a copper seed layer deposition chamber coupled to the transfer chamber without breaking vacuum; and

in the copper seed layer deposition chamber, depositing a copper seed layer over the sidewalls and bottom of the via.

11. The process of claim 10 wherein depositing a barrier layer comprises depositing tantalum.